Field of the Invention

Cross-Reference To Related Applications

This application is a divisional of application No. 09/398,840, filed September 17, 1999, which is now U.S. Patent No. 6,628,159.

On page 15, lines 5-18, please replace the paragraphs as follows:

The structure in Figure 4 is an NFET implementation of the invention. Figure 5 illustrates a PFET implementation, which operates as described above except, capacitor 41 and resistive transistor 42 initiate RC coupling of the gate 45, 145. Element 44 acts as a voltage reference which limits the body potential to the reference voltage V_{ref}. In an ESD event, the RC network couples the gate 45 of the pass transistor 43, 143.

Similarly, Figure 6 illustrates a PFET/NFET switch which includes RC networks 41, 42 which operate as described above. In addition, the structure in Figure 6 includes body limiting devices 60 which limit the body voltage during functional operation. In the example shown in Figure 6, the body limiting devices 60 are coupled to reference voltages of Vref2 = Vdd - ($|V_t|$ + 0.5V) and Vrefy = Vtm + 0.5V for the RC networks. The body limiters 60 can be any devices well known to those ordinarily skilled in the art (e.g., NFET, PFET, etc.) that are used to limit voltage or provide a reference voltage.